# PHASE-LOCKED LOOP CIRCUIT AND DELAY-LOCKED LOOP CIRCUIT

## ABSTRACT OF THE DISCLOSURE

A PLL circuit and a DLL circuit able to stabilize a control voltage within a short time after a phase pull-in operation in each cycle of a reference clock. In a phase comparator, the size of a leading phase or a delayed phase of a feedback signal is detected with respect to a reference clock signa, and pulse signals having pulse widths corresponding to the size are output. A current corresponding to the signals is output from a charge pump circuit to a lag-lead filter, and a control voltage obtained by removing noise of the above output is output from a low-pass filter to a voltage-controlled oscillator. Furthermore, through capacitors, pulse signals are superposed on the control voltage, and a sharp waveform is obtained by correcting blunting of the waveform by the low-pass filter. Due to this, the control voltage is stabilized within a short time after a phase pull-in operation in each cycle of the reference clock signal.